



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/830,092	06/27/2001	Kazutaka Shibata	ROH-037	1091
7590	12/01/2004		EXAMINER	
Mr. Steven M. Rabin c/o RABIN & BERDO, P.C. 1101 14th Street, NW Suite 500 Washington, DC 20005			SONG, MATTHEW J	
			ART UNIT	PAPER NUMBER
			1765	
			DATE MAILED: 12/01/2004	

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/830,092	SHIBATA, KAZUTAKA	
	<b>Examiner</b>	<b>Art Unit</b>	
	Matthew J Song	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1)  Responsive to communication(s) filed on 15 September 2004.

2a)  This action is **FINAL**.                    2b)  This action is non-final.

3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## **Disposition of Claims**

4)  Claim(s) 3,4,6,10,12,17-21 and 26-28 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5)  Claim(s) \_\_\_\_\_ is/are allowed.

6)  Claim(s) 3, 4, 6, 10, 12, 17-21 and 26-28 is/are rejected.

7)  Claim(s) \_\_\_\_\_ is/are objected to.

8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

9)  The specification is objected to by the Examiner.

10)  The drawing(s) filed on \_\_\_\_\_ is/are: a)  accepted or b)  objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)  The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)  All   b)  Some \* c)  None of:

1.  Certified copies of the priority documents have been received.
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)  Notice of References Cited (PTO-892)  
2)  Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3)  Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.  
4)  Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.  
5)  Notice of Informal Patent Application (PTO-152)  
6)  Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/15/2004 has been entered.

### ***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 3, 4, 6, 26, 27 and 28 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 3 recites "bracing the substrate with the back side resin layer while the performing the surface grinding step so as to inhibit warpage of the substrate in lines 13-14". The instant specification is silent to bracing and the mechanism for inhibiting warpage. The instant specification only teaches that for the purposes of grinding uniformly a protective resin uniformly, it is preferable to perform the surface grinding step, note page 30.

4. Claim 26 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 26 recites, surface grinding such that the remaining surface layer has a thickness that is uniform at least within the cutting lines defining the individual pieces cut out of semiconductor devices in the cutting out step" in lines 5-7. The instant specification does not support this limitation.

5. Claim 27 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 27 recites, " step of forming a surface resin layer includes forming the surface layer with uniform thickness in lines 2-3". The instant specification does not support forming a surface layer with uniform thickness.

6. Claim 28 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 28 recites, “ grinding the surface resin layer so that the heights of the plurality of projection electrodes is uniform” in lines 2-3. The instant specification does not support grinding so the heights of the plurality of projection electrodes are uniform.

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 10, 12, and 17-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sekine et al (WO99/09595), where US 6,495,914 is used as an accurate translation, in view of Applicants admitted prior art (Admission) or Frye et al (US 5,898,223).

Sekine et al discloses bare chip devices **47** each including a plurality of semiconductor devices or IC chips with metal bumps **46** provided on the electrodes are placed and bonded on a base substrate **41** this reads on applicant's chip bonding step. Sekine et al also discloses connection posts (projections) **42** connected to electrodes **44** formed by etching, this reads on applicant's electrode forming step. Sekine et al also discloses epoxy resin **48** is filled in the recesses on the base substrate and coated over the projections and bare chip devices. The epoxy resin is flattened in its surface by grinding or polishing so that the connection posts **42**, and the metal bumps on the bare chip devices can be exposed, this reads on applicant's resin sealing step. Sekine et al also discloses the base substrate with module structures is cut along the centers

between the adjacent surrounding walls into individual multi-chip module structures, this reads on applicant's cutting step ('914 col 9, ln 1-55 and Figs 4a-4d). Sekine et al also discloses

Sekine et al discloses a bare chip device **47**, including a plurality of semiconductor devices or IC chips bonded on a base substrate **41**. Sekine et al also discloses projections **42** and electrodes **44**, this reads on applicant's projection electrodes, and an epoxy resin coated over the projections and chips ('914 col 6, ln 5-40). Sekine et al does not disclose a first and second semiconductor chip, such that the first and second semiconductor chip defines a chip-on-chip structure.

In applicants admitted prior art, Admission teaches one of the structures capable of heightening the substantial integration density of a semiconductor device is a chip-on-chip structure. Admission also teaches in a semiconductor device having a chip-on-chip structure, a secondary chip is bonded face-down onto the surface of a primary chip and external connection electrodes are provided on the back side of the primary chip. Admission also teaches such a chip-on-chip structure is advantageous to obtain a high integration density of the elements. Admission also teaches semiconductor chips disposed below other semiconductor chips (page 4 of specification and Fig 19). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Sekine et al's chip device by using the chip-on-chip structure taught by Admission to obtain a high integration density of the elements.

In a method of making a chip-on-chip package, Frye et al teaches conventional chip-on-chip assemblies with chips supported by a chip having interconnection circuits on a support chip and bonding the chips with a solder bump and semiconductor chips disposed below other semiconductor chips (Fig 2 and col 3, 1-67). Frye et al also teaches chip on chip arrangements

offer the advantage of utilizing the surface area of the support chip for interconnection routing (col 3, ln 15-25 and col 3, ln 45-50). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Sekine et al's chip device by using the chip-on-chip structure taught by Frye et al to utilize the surface area of the chip more effectively (col 3, ln 45-50).

Referring to claim 12, Sekine et al and Admission or Sekine et al and Frye et al teaches a plurality of chips and the semiconductor chip is bonded face down onto the solid device with an active surface of the semiconductor chip opposed to the solid device and substrate ('914 Figs 4a-4d).

Referring to claims 18-19, Sekine et al and Admission or Sekine et al and Frye et al teaches grinding the resin to expose the chip devices and projections ('914 col 6, ln 20-30), this reads on applicant's removing a surface layer section of the resin.

Referring to claim 20, Sekine et al and Admission or Sekine et al and Frye et al teaches the rear side of the multi-chip module structure is ground by grinding prior to the cutting step (col 6, ln 35-45).

Referring to claim 21, Sekine et al and Admission or Sekine et al and Frye et al teaches the projection electrodes 42 are formed with a height such that the top end of each projection electrode is between the height of the active surface of the chip and a height of an inactive surface of the chip (Figs 4a-4d).

9. Claims 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Egawa (JP 08-236692), where an English abstract and an English Computer translation (CT) have been provided, in view of Applicants admitted prior art (Admission) or Frye et al (US 5,898,223).

Egawa discloses a hybrid integrated circuit device, this reads on applicant's solid device, a semiconductor chip **16, 17** bonded onto a surface of the solid device, projection electrodes for external connection formed on the surface of the solid device **15**, and a protective resin layer **18,19** for sealing the surface of the solid device with head portions of the projection electrodes thereon exposed.

Egawa does not disclose a first and second semiconductor chip, such that the first and second semiconductor chip defines a chip-on-chip structure.

In applicants admitted prior art, Admission teaches one of the structures capable of heightening the substantial integration density of a semiconductor device is a chip-on-chip structure. Admission also teaches in a semiconductor device having a chip-on-chip structure, a secondary chip is bonded face-down onto the surface of a primary chip and external connection electrodes are provided on the back side of the primary chip. Admission also teaches such a chip-on-chip structure is advantageous to obtain a high integration density of the elements. Admission also teaches semiconductor chips disposed below other semiconductor chips (page 4 of specification and Fig 19). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Sekine et al's chip device by using the chip-on-chip structure taught by Admission to obtain a high integration density of the elements.

In a method of making a chip-on-chip package, Frye et al teaches conventional chip-on-chip assemblies with chips supported by a chip having interconnection circuits on a support chip

and bonding the chips with a solder bump and semiconductor chips disposed below other semiconductor chips (Fig 2 and col 3, 1-67). Frye et al also teaches chip on chip arrangements offer the advantage of utilizing the surface area of the support chip for interconnection routing (col 3, ln 15-25 and col 3, ln 45-50). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Sekine et al's chip device by using the chip-on-chip structure taught by Frye et al to utilize the surface area of the chip more effectively (col 3, ln 45-50).

Referring to claim 12, the combination of Egawa and Admission or the combination of Egawa and Frye et al teaches the semiconductor chip is bonded face down onto the solid device with an active surface of the semiconductor chip opposed to the solid device and substrate (Figs 1-4 of Egawa and Fig 19 of Admission and Fig 2 of Frye et al).

10. Claims 3, 4, 6, 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sekine et al (WO99/09595), where US 6,495,914 is used as an accurate translation and an accurate translation can be provided upon request, in view of Fukasawa et al (US 6,455,920) and Ichikawa (JP 02-031437), where an English Abstract has been provided and an accurate translation can be provided upon request.

Sekine et al discloses all of the limitations of claim 3, as discussed previously, except a step for forming a back side resin layer on a back side of the semiconductor substrate and removing a back side resin through polishing or grinding from the semiconductor substrate.

In a method of forming a semiconductor device, Fukasawa et al teaches a semiconductor device **20A** with a resin layer **41** provided on the rear surface of the semiconductor chip.

Fukasawa et al teaches the semiconductor chip is improved and problem damages in the bottom surface of the chip at the time of dicing the semiconductor wafer **51** into individual chips is eliminated (col 17, ln 35 to col 18, ln 67 and Figs 23-26). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify to modify Sekine et al with Fukasawa et al's resin layer on the bottom of the chip to eliminate damage to the bottom of the semiconductor chip during dicing.

The combination of Sekine et al and Fukasawa et al does not teach a back side grinding step of thinning the semiconductor substrate by removing the back side resin through polishing or grinding, from the semiconductor substrate.

In a method of packing a semiconductor chip, Ichikawa teaches a semiconductor chip is sealed in resin **21** and the rear side of the chip is subjected to grinding for a reduction in the packaging height. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify to modify the combination of Sekine et al and Fukasawa et al with Ichikawa's grinding of a resin layer to reduce the height and enhance the packaging density.

Referring to claim 3, the combination of Sekine et al, Fukasawa et al and Ichikawa teaches a step of forming a surface resin layer **48** ('914), a back side resin layer **41** ('920) and a back side grinding step ('437) and further polishing the back side of the semiconductor ('914 col 6, ln 35-40). It is also noted that further polishing is not patentable because splitting of one step into two, where the processes are substantially identical or equivalent in terms of function, manner and result was held to be not patentably distinguish the processes (Ex Parte Rubin 128 USPQ 159). The combination of Sekine et al, Fukasawa et al and Ichikawa teaches forming

projections 43 ('914). The combination of Sekine et al, Fukasawa et al and Ichikawa teaches grinding or polishing ('914 col 6, ln 20-30).

The combination of Sekine et al, Fukasawa et al and Ichikawa is silent to the order of processing steps. The transposition of process steps where the processes are substantially identical or equivalent in terms of function, manner and result was held to be not patentably distinguish the processes ((*Ex Parte Rubin* 128 USPQ 159) and MPEP 2144.04).

The combination of Sekine et al, Fukasawa et al and Ichikawa is silent to the surface resin and the backside resin are substantially the same thickness. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Sekine et al, Fukasawa et al and Ichikawa by optimizing the thickness of the resin layer by conducting routine experimentation to obtain same.

The combination of Sekine et al, Fukasawa et al and Ichikawa is silent to bracing the substrate with the back side resin layer while performing the surface grinding step so as to inhibit warpage of the substrate. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Sekine et al, Fukasawa et al and Ichikawa to perform the surface grinding step first; therefore the bracing the substrate with the backside resin layer would have naturally flowed from the suggestion of the prior art. The fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

Referring to claim 4, the combination of Sekine et al, Fukasawa et al and Ichikawa teaches cutting the substrate after grinding ('914, col 6, ln 30-45).

Referring to claim 6, the combination of Sekine et al, Fukasawa et al and Ichikawa teaches the projections are embedded in the resin layer ('914 col 6, ln 5-40 and Figs 4a-4d).

Referring to claim 26, the combination of Sekine et al, Fukasawa et al and Ichikawa teaches cutting along the centers between the adjacent shield walls after grinding ('914 col 8, ln 40-60), this reads on applicant's cutting along cutting lines after completing the back side grinding step. The combination of Sekine et al, Fukasawa et al and Ichikawa is silent to polishing or grinding the surface resin layer such that the remaining surface layer has a thickness that is uniform. Uniformity is well known in the semiconductor art to be required to increase yield, which is desirable. Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Sekine et al, Fukasawa et al and Ichikawa by polishing or grinding the surface resin layer such that the remaining surface layer has a thickness that is uniform because increased uniformity is desirable in semiconductor manufacturing to increase yield.

Referring to claims 27 and 28, the combination of Sekine et al, Fukasawa et al and Ichikawa is silent to the surface resin layer is formed with uniform thickness and grinding the surface resin layer so that the heights of the plurality of projection electrodes is uniform. Uniformity is well known in the semiconductor art to be required to increase yield, which is desirable. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Sekine et al, Fukasawa et al and Ichikawa by forming a surface resin layer with uniform thickness and grinding the surface resin layer so that the heights of the plurality of projection electrodes is uniform because increased uniformity is desirable in semiconductor manufacturing to increase yield.

***Response to Arguments***

11. Applicant's arguments with respect to claims 3, 4, 6, 10, 12, 17-21 and 26-28 have been considered but are moot in view of the new ground(s) of rejection.

12. Applicant's arguments filed 9/15/2004 have been fully considered but they are not persuasive.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a wafer level basis (pg 8)) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant's argument that the prior art does not teach first chips and second chips therebelow is noted but is not found persuasive. Frye et al (US 5,898,223) teaches a first chip **12, 13** and a second chip **11** therebelow (Fig 1 and Fig 2). Admission teaches a first chip **102** and a second chip **101** therebelow in Fig 19.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a plurality of separate chip-on-chip devices are formed on a wafer level basis, so that individual separate chip-on-chip devices can be produced therefrom (pg 9)) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification

are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant's argument that Frye and Admission are unrelated to chip-on-chip manufacturing is noted but is not found persuasive. Frye et al teaches interconnection layouts for chip-on-chip packages (Abstract) and Admission teaches chip-on-chip structures for heightening integration density.

Applicant's argument that the ordering is critical is noted but is not found persuasive. The primary difference between the prior art and the instantly claimed invention is that the prior art is silent to the order of the process step and the instant claimed invention requires surface grinding followed by backside grinding. MPEP 2144.04 states selection of any order of performing process steps is *prima facie* obvious in the absence of new or unexpected results. Applicant has not demonstrated the order of step produces new or unexpected results. Applicant has merely cited portion of the instant specification, which states that the claimed order is preferable without any experimental data to show a new or unexpected result. Applicant is also reminded that the instant specification also teaches the reversed order can be performed (pg 24), which would lead a person of ordinary skill in the art to believe the claimed order is not critical.

Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. Applicant alleges the order of process steps is critical without providing evidence show the claimed process produces new or unexpected results.

***Conclusion***

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Takebashi et al (JP 59-092536) teaches applying a resin to a substrate and polishing (Abstract).

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew J Song whose telephone number is 571-272-1468. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew J Song  
Examiner  
Art Unit 1765

ROBERT KUNEMUND  
PRIMARY EXAMINER

MJS

